Notice of Allowability	Application No.	Applicant(s)	
	10/662,063	AMER, MAHER	
	Examiner	Art Unit	
	Venkatesh Haliyur	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/26/2007*.

2. ☒ The allowed claim(s) is/are *1-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Allowable Subject Matter

1. The following is an examiner's statement of reasons for allowance:

   Claims 1-25 are allowed over prior art.

   The prior art of record fails to teach and render obvious the limitations as amended in the independent claims 1,10,16, and the dependent claims 2-9, 11-15,17-25.

2. OFDM is fast gaining popularity in broadband standards and high-speed wireless LAN standards such as the IEEE 802.11a. In practice, the most efficient way to generate the sum of a large number of sub-carriers is by using the Inverse Fast Fourier Transform (IFFT). At the receiver side, a fast and efficient implementation of the well-known Discrete Fourier transform (DFT) function called the Fast Fourier Transform (FFT) can be used to demodulate all the sub-carriers. All sub-carriers differ by an integer number of cycles within the FFT integration time, which ensures the orthogonality between different sub-carriers. Several choices are available for implementing an OFDM modem: digital signal processing (DSP) based implementation, DSP-based implementation with hardware accelerators or a complete ASIC implementation. High performance digital signal processors

(DSPs) are widely available in the market today. The computation intensive and time critical functions that were traditionally implemented in hardware are nowadays being implemented in software running on these processors. However, a DSP-based implementation of an OFDM modem has the disadvantage of not being very optimum in terms of chip area occupied and power consumption.

Applicant's invention overcomes limitations incurred with a DSP-based implementation with an ASIC-based approach providing lower gate count and hence, lower cost and lower power consumption. The claimed invention in the instant application advantageously implements an FFT/IFFT engine entirely in ASIC technology so that each of the functional blocks of the FFT/IFFT engine be mapped onto dedicated, parallel hardware resources thereby avoiding the difficult programming and optimization challenges of scheduling time-critical operations through a single DSP core.

According to one embodiment of the present invention, a system for performing an N-point FFT/IFFT operation is provided comprising an input module for receiving a plurality of inputs in parallel and for combining said inputs after applying a multiplication factor to each of said inputs, at least one multiplicand generator for providing multiplicands to said system, at least two multiplier modules for performing complex multiplications, at least one of said multiplier

modules receiving an output of said input module, each of said multiplier modules receiving multiplicands from said at least one multiplicand generator, at least one of said multiplier modules receiving an output of another multiplier module, a map module for receiving outputs of all of said at least two multiplier modules, said map module selecting and applying a multiplication factor to each of said outputs of said at least two multiplier modules, said map module generating multiple outputs and an accumulation module for receiving and accumulating said multiple outputs of said map module.

In a preferred implementation of the present invention, an optimized hardware configuration comprising 3 complex multipliers is used to compute a 64-point FFT/IFFT operation in 64 clock cycles. Advantageously, the total number of clock cycles required to complete the FFT/IFFT operation is minimized while at the same time minimizing the number of complex multipliers needed.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Venkatesh Haliyur whose telephone number is 571-272-8616. The examiner can normally be reached on Monday thru Friday 8:30AM to 4:30PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Venkatesh Haliyur

Patent Examiner

09/10/07

JAY K. PATEL
SUPERVISORY PATENT EXAMINER